IN THE CLAIMS

1-13. canceled

14. (currently amended) A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a non-return to zero (NRZ) data stream, an input to accept threshold values, and outputs to provide bit estimates responsive to a plurality of voltage threshold levels;

a non-causal circuit having inputs to accept bit estimates from the multi-threshold decision circuit, the non-causal circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate determined in response to the non-causal bit value comparisons; [[and,]]

a threshold circuit having an input to accept bit values from the non-causal circuit, an input to accept the NRZ data stream, and outputs to supply threshold values to the multi-threshold circuit that are adjusted in response to asymmetric noise in the NRZ data stream; and,

wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply the current, first bit, estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit

value, the present decision circuit comparing the first bit estimate to both the second bit value, received prior to the first bit estimate, and the third bit value, received subsequent to the first bit estimate, the present decision circuit having an output to supply the first bit value determined in response to comparing the first bit estimates to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

15. canceled

16. (currently amended) The system of claim [[15]] 14 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the NRZ data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the NRZ data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the NRZ data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the NRZ data stream input has an approximately equal probability of being a "0" value as a "1" value.

17. (currently amended) The system of claim 16 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" [[if]] when both the second and third bit value are "0" values;

a first bit value of "0" [[if]] when only one of the second and third bit values is a "0" value; and,

a first bit value of "0" [[if]] when both the second and third bit values are a "1".

18. (currently amended) The system of claim 17 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" [[if]] when both the second and third bit value are "1" values;

a first bit value of "1" [[if]] when only one of the second and third bit values is a "1" value; and,

a first bit value of "1" [[if]] when both the second and third bit values are a "0".

19. (previously presented) The system of claim 18 wherein the threshold circuit includes:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data

stream, the first threshold generator tracking the NRZ data stream input voltage when the second and third bit values both equal "1" and maintaining a long-term average of the tracked NRZ data stream input voltage, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average.

20. (previously presented) The system of claim 19 wherein the threshold circuit includes:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream input, the second threshold generator tracking the NRZ data stream input voltage when the second and third bit values both equal "0" and maintaining a long-term average of the NRZ data stream input voltage, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

21. (currently amended) The system of claim 20 wherein the threshold circuit includes:

a third threshold generator having an input to accept the NRZ data stream input, the third threshold generator measuring [[the]] a mean voltage of the NRZ data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

22. (original) The system of claim 21 wherein the third threshold generator measures the mean voltage by measuring the NRZ data stream input voltage for all bit sequences.

23. (previously presented) The system of claim 21 wherein the third threshold generator has an input to accept the output of the non-causal circuit, and wherein the third threshold generator measures the mean voltage by measuring the NRZ data stream input voltage when the second bit value does not equal the third bit value.

24. (previously presented) The system of claim 21 wherein the multi-threshold circuit accepts an NRZ data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply a stream of corrected data bits; and,

wherein the third threshold generator has an input to accept the stream of corrected bits from the FEC circuit, the third threshold generator offsetting the third threshold (Vopt) in response to comparing the first bit values to corresponding corrected bit values.

25. (original) The system of claim 24 wherein the third threshold generator tracks the number of corrections in the first bit when the first bit is determined to be a "1" value and offsets the third threshold (Vopt) to minimize the number of corrections.

26. (original) The system of claim 25 wherein the third threshold generator has an output to supply offsets proportional to the offset applied to the third threshold;

wherein the first threshold generator has an input to accept the offset from the third threshold generator, and in response supplies an offset first threshold value; and,

wherein the second threshold generator has an input to accept the offset from the third threshold generator, and in response supplies an offset second threshold value.

27. (original) The system of claim 26 wherein the third threshold generator supplies offsets equal to the offset applied to the third threshold.

28. (currently amended) The system of 21 wherein the third threshold generator has an input to accept the output of the non-causal circuit, and wherein the third threshold generator tracks [[the]] a ratio of first bit "1" values to first bit "0" values and applies an offset to the third threshold (Vopt) to make the tracked ratio approximately equal to one.

29. (original) The system of claim 28 wherein the third threshold generator has an output to supply the offset;

wherein the first threshold generator has an input to accept the offset, and in response supplies an offset first threshold value; and,

wherein the second threshold generator has an input to accept the offset, and in response supplies an offset second threshold value.

30. (original) The system of claim 16 wherein the present decision circuit supplies approximately an equal number of "0" and "1" first bit values in response to establishing the first, second, and third thresholds in the first, second, and third threshold generators, respectively.

31. (new) A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a serial data stream, an input to accept threshold values, and outputs to provide bit estimates responsive to a plurality of voltage threshold levels;

a non-causal circuit having inputs to accept bit estimates from the multi-threshold decision circuit, the non-causal circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate determined in response to the non-causal bit value comparisons;

a threshold circuit having an input to accept bit values from the non-causal circuit, an input to accept the serial data stream, and outputs to supply threshold values to the multi-threshold circuit that are adjusted in response to asymmetric noise in the serial data stream; and,

wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply the current, first bit, estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, received prior to the first bit estimate, and the third bit value, received subsequent to the first bit estimate, the present decision circuit having an output to supply the first bit value determined in response to comparing the first bit estimates to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

32. (new) The system of claim 31 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the serial data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the serial data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the serial data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the serial data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the serial data stream, an input establishing a third threshold (Vopt), and an output to

provide a signal when the serial data stream input has an approximately equal probability of being a "0" value as a "1" value.

33. (new) The system of claim 32 wherein the future decision circuit supplies a first bit estimate for a serial data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" when both the second and third bit value are "0" values;

a first bit value of "0" when only one of the second and third bit values is a "0" value; and,

a first bit value of "0" when both the second and third bit values are a "1".

34. (new) The system of claim 33 wherein the future decision circuit supplies a first bit estimate for a serial data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" when both the second and third bit value are "1" values;

a first bit value of "1" when only one of the second and third bit values is a "1" value; and,

a first bit value of "1" when both the second and third bit values are a "0".

35. (new) The system of claim 34 wherein the threshold circuit includes:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the serial data stream, the first threshold generator tracking the serial data stream input voltage when the second and third bit values both equal "1" and maintaining a long-term average of the tracked serial data stream input voltage, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average;

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the serial data stream input, the second threshold generator tracking the serial data stream input voltage when the second and third bit values both equal "0" and maintaining a long-term average of the serial data stream input voltage, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average; and,

a third threshold generator having an input to accept the serial data stream input, the third threshold generator measuring a mean voltage of the serial data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

36. (new) The system of claim 35 wherein the multi-threshold circuit accepts a serial data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response

to the decoding, the FEC circuit having an output to supply a stream of corrected data bits; and,

wherein the third threshold generator has an input to accept the stream of corrected bits from the FEC circuit, the third threshold generator offsetting the third threshold (Vopt) in response to comparing the first bit values to corresponding corrected bit values.

(new) A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a serial data stream, an input to accept threshold values, and outputs to provide a plurality of bit estimates responsive to a plurality of voltage threshold levels;

a non-causal circuit having inputs to accept the bit estimates from the multi-threshold decision circuit and an output to supply a first bit value for a current clock cycle in response to comparing a first bit estimate for the current clock cycle to bit values determined in non-current clock cycles;

a threshold circuit having an input to accept the first bit values from the non-causal circuit, an input to accept the serial data stream, and outputs to supply threshold values to the multi-threshold circuit that are adjusted in response to asymmetric noise in the serial data stream; and,

wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply the first bit estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimates, third bit values, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, determined for a clock cycle prior to the current clock cycle, and the third bit value, determined for a clock cycle subsequent to the current clock cycle, the present decision circuit having an output to supply the first bit value determined in response to comparing the first bit estimate to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

38. (new) The system of claim 37 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the serial data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the serial data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the serial data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the serial data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the serial data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the serial data stream input has an approximately equal probability of being a "0" value as a "1" value.

39. (new) The system of claim 38 wherein the future decision circuit supplies a first bit estimate for a serial data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" when both the second and third bit value are "0" values;

a first bit value of "0" when only one of the second and third bit values is a "0" value; and,

a first bit value of "0" when both the second and third bit values are a "1".

40. (new) The system of claim 39 wherein the future decision circuit supplies a first bit estimate for a serial data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" when both the second and third bit value are "1" values;

a first bit value of "1" when only one of the second and third bit values is a "1" value; and,

a first bit value of "1" when both the second and third bit values are a "0".

41. (new) The system of claim 40 wherein the threshold circuit includes:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the serial data stream, the first threshold generator tracking the serial data stream input

voltage when the second and third bit values both equal "1" and maintaining a long-term average of the tracked serial data stream input voltage, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average;

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the serial data stream input, the second threshold generator tracking the serial data stream input voltage when the second and third bit values both equal "0" and maintaining a long-term average of the serial data stream input voltage, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average; and,

a third threshold generator having an input to accept the serial data stream input, the third threshold generator measuring a mean voltage of the serial data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

42. (new) The system of claim 41 wherein the multi-threshold circuit accepts a serial data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply a stream of corrected data bits; and,

wherein the third threshold generator has an input to accept the stream of corrected bits from the FEC circuit, the third threshold

generator offsetting the third threshold (Vopt) in response to comparing the first bit values to corresponding corrected bit values.